REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-76 remain in the application. Claims 1-38 are subject to examination and claims 39-76 have been withdrawn from examination. Claims 77 and 78 have been canceled.

In item 3 on page 2 of the above-identified Office Action, claims 1-7, 10-11, 13-26, 29-30, 32-38, 77, and 78 have been rejected as being unpatentable over Moore et al. (U.S. 6,598,148) (hereinafter "Moore") in view of Freitag et al. (U.S. 6,237,054) (hereinafter "Freitag) under 35 U.S.C. § 103(a).

It is noted that although the rejection inadvertently mentions claim 77 and 78, these claim have been previously canceled as noted above.

In item 20 on page 9 of the above-identified Office Action, claims 8, 9, 12, 27, 28, and 31 have been rejected as being unpatentable over Moore in view of Freitag and further in view of Takahashi et al. (U.S. 5,825,878) (hereinafter "Takahashi") under 35 U.S.C. § 103(a).

Moore discloses a microprocessor integrated circuit having a processing unit located on an integrated circuit substrate. The processing unit operates according to a predefined set of program instructions which are stored in an instruction register. The integrated circuit also has a memory for storing information provided by the processing unit. The substrate also has a ring oscillator thereon. The microprocessor 50 multiplexes the address/data bus by using a feedback to allow the processor to adjust memory bus timing to be fast with small loads and slower with large loads. The output enable line 152 from the microprocessor 50 is connected to all the memories 150 on the circuit board and the loading on the enable line 152 to the microprocessor 50 is directly related to the number of memories 150 connected. The microprocessor monitors how rapidly line 152 goes high after a read and thus, is able to determine when the data hold time has been satisfied and place the next address on the bus. The microprocessor generates the system clock and clock circuit 430 tests process performance. The clock is disposed on the same chip as the microprocessor. There is no apparent disclosure in Moore of the interface connection between the intelligent core (shown as microprocessor 11 in the present application) and the various internal and external peripheral units and the memory devices with the structurable hardware unit (shown as SLE layer 12 in the present application) being

configured as recited in the instant claims. It is not at all apparent from the disclosure in Moore that there is an independent access according to the present invention. According to the present invention, the layer 12 can transfer data from and to the memory devices independently, that is, without the participation of the microprocessor, which is not shown in Moore. Nor does Moore disclose a NAND or a sub-block configured as a state machine for central sequence control as recited in instant dependent claim 12. Moreover, the Examiner acknowledges that Moore is deficient in that it does not disclose a hardware unit that can be configured as recited in the claims and to evaluate and process data and/or signal received as set forth in the instant claims of the above identified application.

Freitag discloses a network interface unit with a microcontroller having multiple blocks of programmable logic that are variably ocnfigured to perform selected functions. An execution unit includes a processor core and multiple configurable logic blocks coupled to the processor core. Each of the blocks includes programmable logic which may be PLA or PAL circuitry or FPGA circuitry.

Takahashi discloses a secure embedded memory management unit for a microprocessor for data transfer from an external

memory. While Takahashi shows the use of NAND gates 56, 60, there is no apparent reason why one skilled in the art would necessarily combine Takahashi with Moore other than through hindsight. There is no teaching or suggestion in Moore that Moore requires or for that matter would even want to use the NANDs shown in Takahashi. Or that Moore has need or would want to use a sub-block configured as a state machine for central sequence control. And even if the combination of Takahashi with Moore is proper, which it is not, the resulting unit still would not result in the claimed invention. Takahashi does not overcome the deficiencies of Moore. The Examiner's statements that it would have been obvious to combine Takahashi with Moore "because it would provide a high performance microprocessor that can be directly connected to memory controller" is nothing more than wishful thinking on the part of the Examiner. It is apparent that the Examiner has recognized the deficiencies of the primary Moore reference relative to the claimed invention and as a consequence then has sought those particular features in the prior art without any motivation or particular suggestion in Moore.

It is well settled that almost all claimed inventions are but novel combinations of old features. The courts have held in this context, however, that when "it is necessary to select elements of various teachings in order to form the claimed

invention, we ascertain whether there is any suggestion or motivation **in the prior art** to make the selection made by the applicant". Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985) (emphasis added). "Obviousness can not be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination". In re Bond, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). "Under Section 103 teachings of references can be combined **only** if there is some suggestion or incentive to do so." ACS Hospital Systems, Inc. v. Montefiore Hospital et al., 221 USPQ 929, 933, 732 F.2d 1572 (Fed. Cir. 1984) (emphasis original). "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be **'clear and particular.'**" Winner Int'l Royalty Corp. v. Wang, 53 USPQ2d 1580, 1587, 202 F.3d 1340 (Fed. Cir. 2000) (emphasis added; citations omitted); Brown & Williamson Tobacco Corp. v. Philip Morris, Inc., 56 USPQ2d 1456, 1459 (Fed. Cir. Oct. 17, 2000). Applicants believe that there is no "clear and particular" teaching or suggestion in Moore to incorporate the features of Freitag and/or Takahashi, as proposed by the Examiner. The Examiner merely has made general statements that it would be obvious to combine Moore and Freitag and Moore and Freitag with Takahashai and that the motivations are

"to implement programmable logic circuitry to implement one of many possible communication protocol" and "to provide high performance microprocessor that can be directly connected to memory controller." These are merely general statements by the Examiner without any specific basis in the primary Moore reference as to why one skilled in the art would even want to modify Moore in the first instance.

In establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Int. 1985). To this end, the requisite motivation must stem from some teaching, suggestion, or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in the art and not from the ***applicant's*** disclosure. See, for example, Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1439 (Fed. Cir. 1988), *cert. den.*, 488 U.S. 825 (1988). The Examiner has not provided the requisite reason why one of ordinary skill in the art would have been led to modify Moore or to combine Moore's and Freitag's and Takahashi's teachings to arrive at the claimed invention.

Applicant respectfully believes that any teaching, suggestion, or incentive possibly derived from the prior art is only present with hindsight judgment in view of the instant application. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps.... The references **themselves** must provide some teaching whereby the applicant's combination would have been obvious." In re Gorman, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991) (emphasis added). Here, no such teaching is present in the cited references.

The references do not show "a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units...and said structurable hardware unit being configured so that it can be configured like a configuration of field-programmable logic arrangements such as PLAs, GLAs, PLDs, FPGAs and to evaluate and process data and/or signals received thereby " as recited in claim 1 of the instant application. Independent claim 20 contains similar limitations.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either

show or suggest the features of claim 1 or 20. Claims 1 and 20 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 20.

Additionally, the references do not disclose the claimed limitations of dependent claims 8, 10, 12, and of dependent claims 27, 29, and 31.

In view of the foregoing, reconsideration and allowance of claims 1-38 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required for this paper, petition for extension is herewith made.

Appl. No. 09/816,933
Amdt. dated 5/2/06
Reply to Office action of 3/2/06

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Werner H. Stemer (34,956)

FDP/bb

May 2, 2006

Lerner Greenberg Stemer, LLP
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.